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**\*BIBDATASHEET\***

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**CONFIRMATION NO. 7327**

SERIAL NUMBER 10/527,569	FILING OR 371(c) DATE 03/10/2005 RULE	CLASS 324	GROUP ART UNIT 2829	ATTORNEY DOCKET NO. NL02 0843 US
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**APPLICANTS**

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**\*\* CONTINUING DATA \*\*\*\*\***

This application is a 371 of PCT/IB03/03429 08/04/2003

**\*\* FOREIGN APPLICATIONS \*\*\*\*\***

EUROPEAN PATENT OFFICE (EPO) 02078785.9 09/13/2002

Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY NETHERLANDS	SHEETS DRAWING 3	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 3
35 USC 119 (a-d) conditions <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Allowance				
Verified and Acknowledged Examiner's Signature _____ Initials _____				

**ADDRESS**

24738

**TITLE**

Reduced chip testing scheme at wafer level

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